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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,325	12/01/2003	Fwu-Iuan Hshieh	GS 152 D1	2691

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EXAMINER	
LOKE, STEVEN HO YIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/725,325	HSHIEH ET AL.	
	Examiner	Art Unit	
	Steven Loke	2811	AU

-- Th MAILING DATE of this communication appears on the cover sheet with th correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-20,22-24,26 and 27* is/are rejected.

7)☒ Claim(s) *21 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/1/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The title should direct to a method of making the semiconductor device.

2. The abstract of the disclosure is objected to because it should direct to a method of making the semiconductor device. Correction is required.

3. Claims 18-27 are objected to because of the following informalities: Claim 18, line 7, the phrase "said epitaxial region" has no antecedent basis. Claim 19, line 3, the word "dopant" is unclear whether it is being referred to the dopant in line 2 of claim 19. Claim 24, line 1, the phrases "said steps" and "said trenches" have no antecedent basis. Appropriate correction is required.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 18-20, 22, 23 and 26 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Yang (IDS filed on 12/1/03).

In regards to claim 18, Yang shows all the elements of the claimed invention in figs. 2a to 2l. It discloses a method of forming a trench MOSFET device, comprising: providing a substrate [31] of a first conductivity type (n-type); depositing an epitaxial layer [32] of said first conductivity type over said substrate, said epitaxial layer having a lower majority carrier concentration than said substrate; forming a body region [35] of a second conductivity type (p-type) within an upper portion of said epitaxial layer; etching

a trench [70] extending into said epitaxial layer from an upper surface of said epitaxial layer, said trench extending to a greater depth from said upper surface of said epitaxial layer than does said body region; forming a doped region [39] of said first conductivity type between a bottom portion of said trench and said substrate, said doped region having a majority carrier concentration that is lower than that of said substrate and higher than that of said epitaxial layer (col. 4, lines 12 to 28); forming an insulating layer [33d] lining at least a portion of said trench; forming a conductive region [40] within said trench adjacent said insulating layer; and forming a source region [36] of said first conductivity type within an upper portion of said body region [35] and adjacent said trench.

In regards to claim 19, Yang further discloses said step of forming said doped region [39] comprises: (a) implanting a dopant of said first conductivity type into said epitaxial layer [32]; and (b) diffusing dopant of said first conductivity type at elevated temperature (col. 3, lines 62 to 65).

In regards to claim 20, Yang further discloses said dopant is diffused until the doped region spans more than 50% of the distance from said trench bottom to said substrate.

In regards to claim 22, Yang further discloses said first conductivity type is n-type conductivity and said second conductivity type is p-type conductivity.

In regards to claim 23, Yang further discloses said dopant is phosphorous.

In regards to claim 26, Yang inherently discloses said trench MOSFET device is a silicon device.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yang in view of Bulucea et al. (IDS filed on 12/1/03).

In regards to claim 27, Yang further discloses forming a metallic source contact adjacent an upper surface of the source region [36].

Yang differs from the claimed invention by not showing forming a metallic drain contact adjacent said semiconductor substrate, and forming a metallic gate contact adjacent an upper surface of said conductive region remote from said source region.

Bulucea et al. show forming a drain contact [45] adjacent the semiconductor substrate [23], and forming a metallic gate contact [43a] adjacent an upper surface of said conductive region [36a] remote from said source region [28] in fig. 31A.

Since both Yang and Bulucea et al. teach a vertical MOSFET with a drain region and a gate electrode, it would have been obvious to have the drain contact and the metallic gate contact of Bulucea et al. in Yang because they provide connection between the semiconductor device and the external circuit.

Bulucea et al. differ from the claimed invention by not showing the drain contact is a metallic layer. It would have been obvious for the drain contact is a metallic layer because it is a conventional drain contact material.

8. Claims 18 and 24 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Blanchard (IDS filed on 12/1/03).

In regards to claim 18, Blanchard shows all the elements of the claimed invention in figs. 4a to 4j. It discloses a method of forming a trench MOSFET device, comprising: providing a substrate [11] of a first conductivity type (n-type); depositing an epitaxial layer [12] of said first conductivity type over said substrate, said epitaxial layer having a lower majority carrier concentration (10^{15} atoms/cm^3) than said substrate (10^{19} atoms/cm^3); forming a body region [15] of a second conductivity type (p-type) within an upper portion of said epitaxial layer; etching a trench [36] extending into said epitaxial layer from an upper surface of said epitaxial layer, said trench extending to a greater depth from said upper surface of said epitaxial layer than does said body region; forming a doped region [39] of said first conductivity type between a bottom portion of said trench and said substrate, said doped region having a majority carrier concentration ($5x10^{17}$ atoms/cm^3) that is lower than that of said substrate and higher than that of said epitaxial layer; forming an insulating layer [40] lining at least a portion of said trench; forming a conductive region [42] within said trench adjacent said insulating layer; and forming a source region [16] of said first conductivity type within an upper portion of said body region [15] and adjacent said trench.

In regards to claim 24, Blanchard further discloses said steps of forming said trench and forming said doped region comprise: (a) forming a trench mask [35] on said epitaxial layer; (b) etching said trench through said trench mask; (c) implanting a dopant of said first conductivity type through said trench mask; and (d) diffusing said dopant of

said first conductivity type at elevated temperature (during the thermal oxidation step to form the gate dielectric [40]).

9. Claims 21 and 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter: The first major difference in the claims not found in the prior art of record is said dopant is diffused until the doped region spans 100% of the distance from said trench bottom to said substrate. The second major difference in the claims not found in the prior art of record is said elevated temperature is provided by a step in which a sacrificial oxide is grown along walls of said trench.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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May 16, 2004

Steven Loke
Primary Examiner